IN THE DRAWINGS:

The attached sheets of drawings include changes to FIGs. 1-2. These sheets replace the original sheets that included FIGs. 1-2.

IN THE CLAIMS:

Please amend claims 1-10 and add claims 20-29 as follows:

1. (Currently Amended) A ~~S~~storage device for a multibus architecture, comprising:

—at least one memory ~~(M)~~ that~~o~~ stores ~~data (d),~~ information ~~and/or addresses;~~,

—a memory connection having ~~(B) including~~ a port ~~(B0)~~ that~~o~~ is connected to the at least one memory ~~(M)~~ and is selectively connected to ~~a first~~ one of a plurality of buses within the ~~(D0) of a~~ multibus architecture ~~(P, D0, D1, R)~~,

~~—wherein~~ at least one data line that communicates with the memory connection ~~(B), the port (B0),~~ and the one of the plurality of ~~first~~ buses to provide information to the memory connection to control the memory~~, where the at least one data line~~(P) ~~have data lines (DL) to transmit the data (d), and, as required, transmit addresses (a) and/or control information to control the memory (M);~~, and

~~characterized by~~

—a switching device ~~(SW, MTR, CU, ARB, MOD) to~~ that selectively connects the memory connection ~~(B)~~ to one of the plurality of buses ~~(D1, P, R) for a memory access to effect transmission of data, addresses, and/or control~~ to transmit information between the one of the plurality of ~~from or to this~~ buses and the memory.

2. (Currently Amended) The ~~S~~storage device of ~~according to C~~claim 1, further comprising:

a ~~memory specific~~ logic device ~~(L)~~ connected with ~~and~~ an interrupt line ~~(STL) to~~ that transmits an interrupt signal on the interrupt line ~~(st)~~ from the logic device to a processor, ~~system (PU) so as to control the complete system such that by sending~~ where the interrupt signal ~~(st), an~~ interrupt~~sion~~ operation of the processor ~~operation is always triggered~~ for one clock cycle whenever a memory access is to be effected by the memory ~~(M)~~ to two of the plurality of

~~different~~ buses ~~(P, D0, D1, R), or to the memory (M) by these buses,~~ within two successive clock cycles.

3. (Currently Amended) The storage device of ~~according to C~~claim 1, further comprising an analyzer ~~(ARB, CU)~~ connected to ~~on the input side of~~ the memory, that ~~(M) for~~ analyze~~sing~~ addresses on ~~the~~ address lines ~~(AL)~~ that form a part of at least one of the plurality of ~~assigned to the~~ buses ~~and/or the memory~~ for determining ~~memory~~ accesses to the at least one memory, and ~~for appropriately~~ that switche~~sing~~ the switching device ~~(SW)~~ to a corresponding one of the ~~corresponding~~ plurality of buses ~~(P, D0, D1, R)~~.

4. (Currently Amended) The ~~S~~storage device of ~~according to C~~claim 3, where~~in~~ the analyzer ~~(ARB, CU) is designed for~~ analyze~~sing~~ a part of the addresses~~,~~ and ~~for~~ switche~~sing~~ and assigns~~ing~~ a memory access for address segments smaller than a ~~the~~ word width of one of the plurality of ~~a~~ buses ~~transmitting~~ having the addresses ~~or of the address lines (AL)~~.

5. (Currently Amended) The ~~S~~storage device of ~~according to C~~claim 3, further comprising an adjustable separator device~~, specifically a programmably adjustable separator device (MTR) to~~ that stores a memory address of the at least one memory ~~(M)~~ for analysis by the analyzer ~~(ARB, CU)~~.

6. (Currently Amended) The ~~S~~storage device of ~~according to C~~claim 3, where~~in~~ the analyzer further comprises ~~has~~ a common access control device ~~(ARB) to~~ that switches the

switching device ~~(SW)~~, and one comparator ~~(CU) each~~ per each one of the plurality of buses ~~(P, D0, D1, R)~~ to compare the address with the memory address of the at least one memory ~~(M)~~.

7. (Currently Amended) The ~~S~~storage device of ~~according to C~~claim 3, where~~in~~ the analyzer further comprises ~~has~~ a modifier that ~~(MOD) which is designed to~~ processes different ~~data~~ types of information ~~and/or access types which are~~ applied to the modifier ~~(MOD) and/or to a data memory segment of the memory (M)~~ each one of the plurality of buses selectively connected ~~through data lines, subaddress lines, and/or access signal lines (DL, SAL, ACL) selected~~ by the switching device to the modifier ~~(SW) in order to transmit states on the bus lines (DL)~~.

8. (Currently Amended) The ~~S~~storage device of ~~according to~~ claim 1~~7~~, further comprising a ~~or the~~ logic device that provides ~~(L, CU) to issue~~ a block loss signal ~~(BM) through~~ on a signal ~~loss~~ line ~~(BML)~~ to a ~~higher level~~ processor ~~system (PU)~~ in response to a deviation from an ~~the announced and~~ executed data transfers during an~~the~~ access to the at least one memory ~~access~~.

9. (Currently Amended) The s~~S~~torage device of claim 1, where the at least one memory stores information that comprises data~~comprising a plurality of storage devices which is switchably connected to one bus each within a multibus architecture having a plurality of busses (P, D0, D1, R)~~.

10. (Currently Amended) The storage device of claim 1, where the at least one memory stores information that comprises addresses~~Storage system according to Claim 9, which~~

~~particularly in the case of a switch between read access and write access for one of the memories (M) is designed to effect the clock-cycle-based alternating control of different memories (M) by a common high-level processor system (PU).~~

11. (Cancelled)

12. (Cancelled)

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Cancelled)

17. (Cancelled)

18. (Cancelled)

19. (Cancelled)

20. (New) A storage device for use with a bus architecture having a plurality of buses including address, data and control information transmitted on the plurality of buses, the storage device comprising:

a memory;

a switching device that selectively connects the memory with one of the plurality of buses to transmit information on the selected one of the plurality of buses to the memory;

a logic device that provides an interrupt signal on a line to a processor to interrupt operation of the processor whenever an access to the memory is desired by at least one of the plurality of buses; and

an analyzer that analyzes an address on address lines that form a portion of at least one of the plurality of buses, where the analyzer controls the switching device to selectively connect one of the plurality of buses to the memory depending on the address that is analyzed by the analyzer.

21. (New) The storage device of claim 20, further comprising a separator device that stores an address of the memory for analysis by the analyzer.

22. (New) The storage device of claim 20, where the analyzer analyzes a portion of the address on the address lines that form a portion of at least one of the plurality of buses.

23. (New) The storage device of claim 20, where the analyzer further comprises a common access control device that controls the switching of the switching device.

24. (New) The storage device of claim 20, where the analyzer further comprises a modifier that determines the type of information that is provided to the memory for storage thereby.

25. (New) The storage device of claim 24, where the modifier determines the type of information that is provided on the one of the plurality of buses that is connected with the memory by the switching device.

26. (New) The storage device of claim 20, where the memory further comprises a memory connection that facilitates connection of the memory to the information on the one of the plurality of buses selectively connected to the memory connection by the switching device.

27. (New) The storage device of claim 20, where the information stored by the memory comprises data.

28. (New) The storage device of claim 20, where the logic device provides a block loss signal on a line to a processor in response to a deviation from an executed data transfer during an access to the memory.

29. (New) A method for storing data in a memory storage device for use with a bus architecture having a plurality of buses, the method comprising:

selectively connecting the memory storage device with one of the plurality of buses to transmit the information on the selected one of the plurality of buses to the memory;

interrupting operation of a processor whenever an access to the memory is desired by at least one of the plurality of buses; and

analyzing an address on address lines that form a portion of at least one of the plurality of buses and by controlling the selective connection of one of the plurality of buses to the memory depending on the address analyzed by the analyzer.